

ARTICLE

Ge-based Medium Wave Infrared MCT 1280×1024 Focal Plane Detector

Jun Jiang*

Kunming institute of physics, Kunming, Yunnan, 650223, China

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ABSTRACT

Medium-wave HgCdTe thin films grown on germanium-based substrates by molecular beam epitaxy were treated by large area n-on-p injection junction and flip-flop mixing process. The chips interconnected with low-noise and multimodal options readout circuit composed a 1280×1024 Medium-wave Infrared Focal Plane Cooling Detector whose pixel spacing was 15 microns. Its main photoelectric properties are average NETD equivalent to 18.5 mK, non-uniformity equivalent to 7.5%, operability equivalent to 98.97%. The paper also studies the substrate-removal technique on Germanium-based chip, which improves the stability and reliability of detector.

1. Introduction

Infrared technology is a photoelectric conversion technology that converts infrared radiation into identifiable electrical signals. It is one of the key technologies to realize the informatization of high-tech equipment. Infrared detector is the core of infrared technology. Its quality and characteristics determine the performance and level of equipment. Infrared detector has the advantages of long operating distance, good anti-interference, strong ability to penetrate smoke and haze, and can work all day. It has been widely used in military and civil fields.

In recent years, in order to achieve high spatial resolution, large-scale and super large-scale infrared focal plane detector components have attracted great attention. As a megapixel focal plane detector with the typical characteristics of the third generation focal plane, it is widely used in aviation, aerospace and other aspects^[1].

Traditional infrared focal plane detectors mostly use CdZnTe Single crystal wafer with good lattice matching with HgCdTe photosensitive material as epitaxial substrate. However, due to the characteristics of long process cycle, low crystallization rate, small ingot size and low yield of CdZnTe Single Crystal^[2], the price of epitaxial

*Corresponding Author:

Jun Jiang,

Kunming institute of physics, Kunming, Yunnan, 650223, China;

Email: jj.wjy@163.com

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CdZnTe substrate is high. In order to overcome the problems of small size and high chip preparation cost of traditional HgCdTe epitaxial materials, ultra large scale focal plane arrays are prepared by germanium based HgCdTe materials, which have obvious advantages in the preparation of megapixel focal plane detectors.

2. Design and Process Realization of Germanium Based Medium Wave HgCdTe Focal Plane Detector Assembly

2.1 Medium Wave HgCdTe Thin Film Material Molecular Beam Epitaxy on Germanium Based

The epitaxial HgCdTe material on Ge substrate faces many technical challenges, among which the biggest problem is that the lattice mismatch is as high as 14%, which makes the problems such as epitaxial layer crystal direction control, high-density dislocation suppression and surface defect density suppression particularly prominent^[3]. Around these problems, the high-precision calibration and control of growth temperature, substrate material pretreatment technology structure design and growth of composite buffer layer, large area HgCdTe material epitaxy process, HgCdTe material heat treatment technology and other core processes.

The surface state of Ge substrate directly affects the quality of epitaxial layer and the number and size of surface macro defects^[4]. The carbon particles on the surface need to be removed at a high temperature of 1200 °C, which is difficult for MBE equipment, and carbon may form surface macro defects, so how to remove carbon becomes the key of Ge substrate epitaxy. The epitaxial HgCdTe material on Ge substrate also faces many technical challenges. The biggest problem is the serious lattice mismatch, which makes it very difficult to control the crystal orientation of epitaxial layer, suppress high-density dislocations and suppress the density of surface macro defects. Around these problems, through low-temperature oxide layer removal technology, epitaxial layer polarity control technology, atomic layer epitaxy technology The atomic level flat surface is obtained by epitaxy technology at extreme temperature, high temperature annealing technology, crystal deflection angle and increasing surface atomic step density.

At the same time, through a large number of experiments, an effective Ge substrate cleaning and corrosion process was found out. Combined with vacuum low-temperature deoxidation and as monolayer Ge surface passivation process, an atomic level flat surface suitable for epitaxial growth was obtained.

Due to the different crystal properties of germanium

and HgCdTe materials, there is a large defect density. It is necessary to control the interface layer of germanium and HgCdTe through appropriate design and process, control the lattice mismatch and other defects in the interface buffer layer, and suppress the material defects in the HgCdTe photosensitive layer. In the study, HgTe/CdTe alternating structure (20 cycles) was used to improve the EPD of MCT materials. On the composite substrate after the growth of CdTe buffer layer, before the growth of MCT materials, the HgTe/CdTe alternating layer with a long period of 20 cycles was used, as shown in Figure 1.

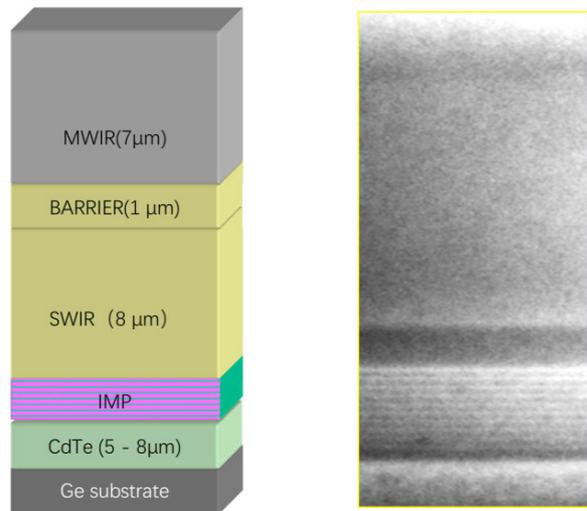


Figure 1. HgTe/CdTe composite buffer layer structure

For the growth of CdTe on large mismatch Ge substrate, there are four main problems: one is that large mismatch causes high dislocation density; The second is that twins are very easy to appear. The research shows that for heteroepitaxy with large lattice mismatch, large mismatch leads to higher surface energy at the interface, The system will deflect and grow in the direction of reducing the energy of the system (i.e. growing towards the crystal surface with low surface energy). The greater the degree of fit, the easier it is to produce polycrystals or twins, resulting in three-dimensional growth mode, which seriously affects the crystal quality. Therefore, the main reason for the formation of twins is the high interface energy caused by large lattice mismatch; the third is the large thermal mismatch between the substrate and CdTe epitaxial layer, which will lead to the generation of stress in the epitaxial layer. The fourth is non-polar To grow polar CdTe on Ge substrate, a non-polar surface needs to be prepared on the surface of clean Ge substrate after high temperature deoxidation.

Large area uniform HgCdTe growth, using Ge single crystal as epitaxial substrate, The lattice mismatch be-

tween Ge single crystal and HgCdTe is large (the mismatch is about 14.6%), so we must epitaxial a layer of CdTe with a certain thickness on Ge as a buffer layer, and then epitaxial HgCdTe. The dislocations on the CdTe surface will extend into the HgCdTe layer grown on it, which will directly affect the HgCdTe crystal quality. In order to determine the relationship between the dislocation density on the CdTe surface and the thickness of the epitaxial layer, we conducted X-ray bicrystal analysis of CdTe epitaxial layers with different thicknesses Swing back curve FWHM measurement and EPD study. It is found that when the thickness is greater than 6 μm , FWHM changed slowly, and the surface EPD value decreased to $(7 \sim 9) \times 10^6\text{cm}^{-2}$, which no longer decreases significantly with the further increase of thickness.

The composite buffer layer with HgTe/CdTe alternating structure is selected. Most of the screw dislocations caused by substrate mismatch are pinned in the alternating structure of 20 cycles. Therefore, the EPD of the subsequently grown multilayer MCT material is significantly controlled, which can reach $2.5 \times 10^6 / \text{cm}^2$ level.

Stable MBE growth temperature is the key factor for the epitaxy of high-quality multilayer HgCdTe films. The growth temperature affects the adhesion coefficient of Hg on the substrate surface and directly determines whether the growth condition is Hg deficient or Hg rich. The number and size of macro defects on the material surface are closely related to the state of Hg. The appropriate growth temperature also determines the crystal quality and corrosion pit density of MCT films.

Through the theoretical simulation of different growth surfaces, the optimal temperature change curve of growth is obtained. Based on this, the heating power is compensated during the growth process, so that the temperature is stable at $\pm 3 \text{ }^\circ\text{C}$ during CdTe growth and $\pm 1 \text{ }^\circ\text{C}$ during MCT growth.

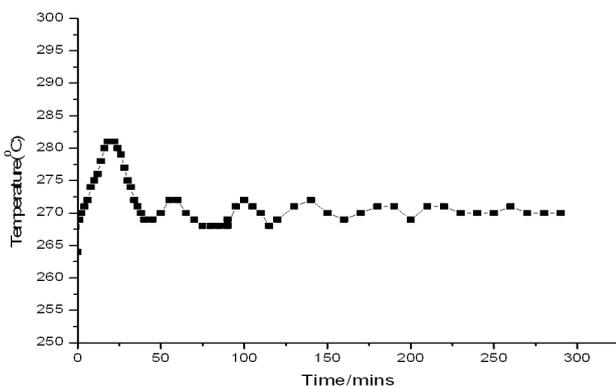


Figure 2. Temperature change curve measured by power compensated CdTe mid infrared thermometer

Through the above research, the properties of Ge based MBE HgCdTe thin films are as follows: half peak width: 90 ~ 110arcsec; Corrosion pit density: $\sim 2.5 \times 10^6/\text{cm}^2$; Surface macro defect density: $\sim 300 / \text{cm}^2 (< 10 \mu\text{m})$.

2.2 Process Realization of Detector Chip

Ge base 1280 \times 1024 HgCdTe photovoltaic detector chip is the core and key of detector module. In the preparation of detector chip, a single-layer p-type large-area HgCdTe material doped with Hg vacancy is used to form the detector photosensitive element array by ion implantation. The plane junction technology is adopted, and the pixel center distance is 15 μm . The structure is shown in Figure 3.

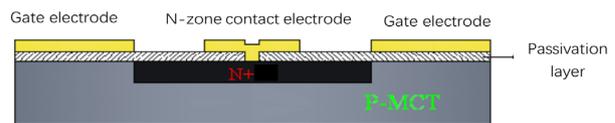


Figure 3. Photosensitive element structure

The research of detector chip is based on mature technologies such as material surface treatment, passivation, ion implantation, high-precision lithography, flip chip interconnection, dry etching and back thinning. It focuses on core processes such as high-performance surface passivation, large-scale high-density and high-reliability interconnection technology.

Good surface passivation process can effectively reduce the surface damage of HgCdTe, reduce the interface state of HgCdTe device surface, reduce the leakage current on the device surface, reduce the surface recombination speed and 1/f noise of HgCdTe device, improve the dynamic resistance and directional breakdown voltage of detector, and improve the performance of device^[5]. Therefore, in the device process, the preparation of dense and high resistance passivation layer is studied. In this paper, the CdTe/ZnS composite passivation film system is adopted. In view of the imbalance between Cd and Te in the ordinary CdTe growth mode, the Te rich CdTe passivation film is obtained by adding high-purity Te technology, which effectively reduces the Hg rich defect state density on the surface of HgCdTe caused by heat treatment process and greatly reduces the dark current of the device. The dynamic resistance of the device is effectively improved. In the passivation process, a CdTe/ZnS composite passivation film with excellent surface roughness and adhesion was prepared by adjusting the RF power, target substrate distance and sample swing angle. The non-uniformity of the passivation film reached $\pm 4.3\%$ in 3-inch samples. It provides a composite passivation film preparation process with better repeatability and consistency for

the preparation of large array HgCdTe devices.

In this paper, flip interconnect optical sensitive array chip and readout circuit (ROIC) are used for electrical connection, as shown in Figure 4. Due to the large scale of the developed array (1280×1024), more than 1.3 million interconnection points need to be welded. In the interconnection technology, not only the electrical and mechanical connection of the interconnection point should be ensured, but also the stress caused by the mismatch of thermal expansion between the detector chip and the silicon readout circuit under the cold and heat cycle should be buffered.

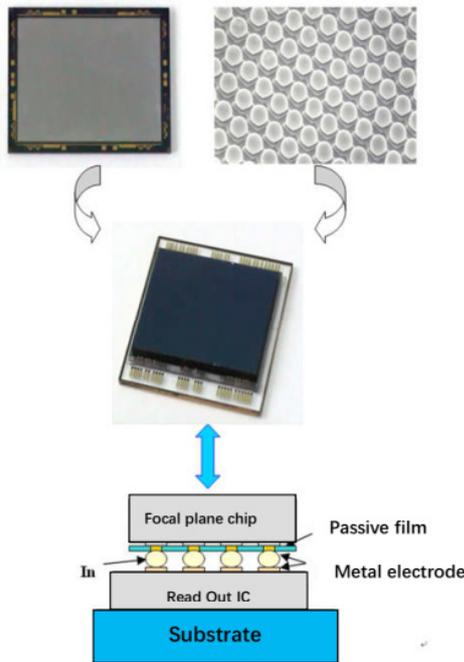


Figure 4. Schematic diagram of flip chip interconnection of focal plane detector

This paper focuses on solving the interconnection reliability between detector chip and readout circuit, improving the growth and molding process of indium column, strictly controlling the parallelism between silicon readout circuit and HgCdTe chip, and ensuring the high consistency of indium column; Secondly, the best process parameters for flip chip welding of various thickness chips, indium column height and large-scale chips are found out. After flip chip welding, epoxy glue is injected between the readout circuit and the chip to enhance the welding strength and effectively fill the gap between them. At present, the flip chip welding connectivity of indium column reaches 100%.

2.3 Readout Circuit Design

The readout circuit integrates, stores, cell gating, line gating, sample hold and high-speed output the instantaneous signal from the photovoltaic diode. The readout circuit adopts mature 0.35 μm CMOS technology, not only has the ability to realize various functions such as low-noise signal processing and output, but also has good low-temperature operating characteristics. The readout circuit has a variety of working modes, windowing and readout modes to meet different application requirements.

The readout circuit integrates, stores, unit gating, row gating and sample hold the signal (direct injection) from the photovoltaic diode, and adopts two working modes: integration before readout (ITR) and integration while readout (IWR), with optional output channels.

The readout circuit is designed with the window selection function. The circuit can select the window as full window or partial window according to the input signals size and sizeb (see Table 1).

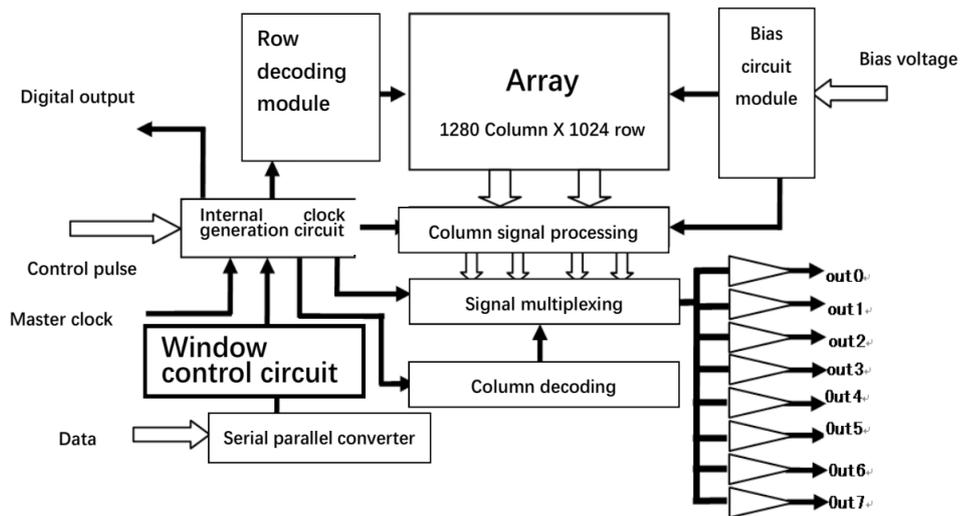


Figure 5. Functional module diagram of readout circuit

Table 1. Selection of working mode

| SIZEA | SIZEB | Format |
|-------|-------|-----------------------|
| 1 | 1 | 1280×1024 (default) |
| 1 | 0 | 1280×960 |
| 0 | 1 | 1024×1024 |
| 0 | 0 | 1280×1024 window mode |

In terms of reducing circuit power consumption, including reasonably setting the size of transistors in the operational amplifier circuit and driving the operational amplifier, through circuit design, the output of the medium wave readout circuit is 4 or 8 channels. When the output is 4 channels, the Output Op Amp of the remaining 4 channels stops working, rather than simply shielding the input/output of the four channel op amp signals with a switch, so as to greatly reduce the power consumption of the circuit.

Due to the increase of readout circuit array, how to improve the consistency of pixel circuit in a limited area has become a difficulty in circuit design. The expansion of readout circuit array will prolong the circuit signal output time, make the capacitor hold signal time longer, and cause the signal uniformity to deteriorate. Therefore, the integral and hold capacitance are appropriately increased in the design. However, due to the limited chip area, the chip area, capacitor charge and discharge time and other factors are comprehensively considered in the design, and the capacitance value is reasonably set, To improve the uniformity of pixel circuit.

2.4 Germanium Based Back Thinning

The focal plane detector in this paper needs to work near the temperature of 80 K. When the refrigerator cools the detector chip from the ambient temperature to the working temperature of the detector chip in a short time, the temperature difference during the cooling process changes by more than 200 K. Due to the mismatch of parameters such as material expansion coefficient, elastic modulus and Poisson’s ratio, the detector chip, readout circuit and Dewar loading substrate, Cause the chip to bear great stress and deformation [6]. In this paper, the structural deformation of dewar cold head detector chip and loading substrate under cooling state is simulated and analyzed, as shown in Figure 6. When the detector chip is cooled to 80 K in a short time, the structural deformation caused by drastic temperature change reaches 10 μm or so. This deformation is mainly caused by the thermal mismatch between the chip and the readout circuit, which is often easy to cause serious consequences such as the rapid increase of bad pixels of the detector chip or chip cracking. Therefore, the back thinning process is a necessary process link for a highly reliable hybrid staring focal plane detector, which can minimize the thermal mismatch between the chip and the readout circuit, improve the reliability of the module, and meet the environmental adaptability requirements of complex and harsh environment applications. Therefore, we must improve the flexibility of the chip itself by thinning the back of the chip, so as to improve the ability of the chip to withstand stress and

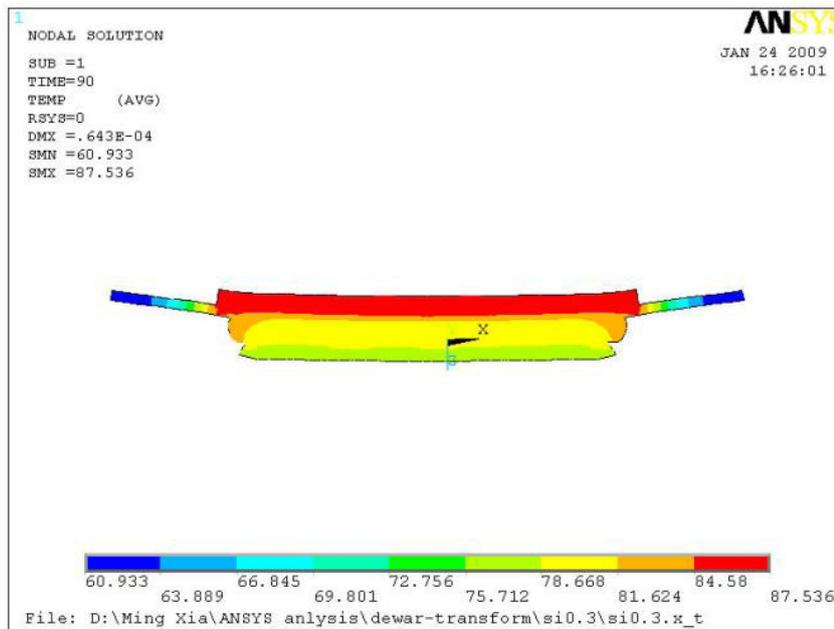


Figure 6. Finite element analysis of chip deformation under cooling state

deformation, and improve the ability of the chip to resist the temperature impact of the refrigerator on and off.

In the process research of Ge based back thinning, a highly reliable filling process is carried out between the light sensitive array chip and the readout circuit. The focal plane chip is filled with filling polymer with good fluidity and stable at low temperature, so as to strengthen the support strength of the chip and further reduce the thermal mismatch of the chip. By means of mechanical turning, the germanium substrate is thinned with low damage and low stress, the whole germanium substrate is completely removed, and the mismatch between germanium substrate and silicon readout circuit caused by inconsistent thermal expansion is reduced. At the same time, the germanium substrate thinned to a certain thickness is finally treated by wet chemical process to remove the damage caused by mechanical thinning, and provide a good interface for the sputtering of back antireflection film.

Through the above mechanical and chemical back subtraction process research, the low damage back subtraction removal of large area array Ge based substrate has been realized. It can be seen from Table 2 that the performance of the device does not decline significantly before and after back substrate removal.

Table 2. Ge base 1280 × Performance comparison of 1024 focal plane detector before and after back substrate removal

| | before | after |
|----------------|---------|---------|
| Bad pixel rate | 1.74% | 1.85% |
| NETD | 22.3 mK | 24.5 mK |
| non-uniformity | 8.1% | 7.9% |

2.5 Dewar Design

The Dewar of the detector assembly is to Ge based medium wave 1280×1024 focal plane detector chip provides an all metal vacuum packaging structure, which can make the detector chip work in a 77 K vacuum environment after matching with the refrigerator. At the same time, Dewar also provides an optical transmission channel for transmitting infrared radiation, which includes the optical window of Ge material, filter and aperture. The filter is coated with a band-pass optical film to limit the transmission of a specific infrared wavelength, and the aperture is used to limit the optical aperture (F#) of the detector, which is usually matched with the imaging lens.

In the design of Dewar, the principles of universality, small volume, light weight and high reliability are fully considered. The all metal integrated structure is adopted. The high-strength and low thermal conductivity thin-

walled metal inner tube is integrated with the refrigerator. The high air tight HTCC ceramic lead ring is directly interconnected with the loading substrate. The electroforming process realizes the manufacture of high-strength ultra-thin aperture. The aperture adopts high-strength ultra-thin multi-layer structure. The aperture not only ensures the optical F# but also increases the multi-layer impurity elimination to aperture improve the cold shielding efficiency. All parts of Dewar adopt strictly controlled surface treatment process to ensure vacuum service life and reliability.

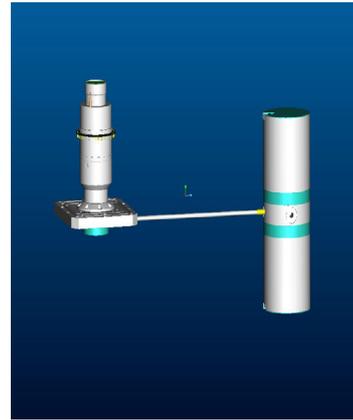


Figure 7. Design structure of Dewar

In order to effectively reduce the background radiation noise, the v adopts a multi-layer anti stray light structure, and the multi-layer structure is also conducive to the improvement of the structural strength of the aperture. Improving the emissivity of the blackened layer on the inner surface of the aperture can improve the ability to absorb secondary and multiple reflected stray light. The emissivity of the blackened coating is higher than 95%, which can minimize the infrared background radiation and improve the detection rate, so as to improve the quality of thermal imaging.

ANSYS and other simulation software are used to analyze the stress and deformation of the cold head structure, optimize the structure, metal coating and contact surface shape of each Dewar part in the cold head laminated structure, determine the selected materials of each part, and ensure the temperature uniformity of the loading surface of the detector. By continuously optimizing and improving the materials and structures of metal negatives, transition blocks and loading substrates, the optimal combination of cold head structure is achieved. The temperature distribution diagram of the cold head before and after the optimization and improvement of the dewar cold head structure. The temperature difference on the loading surface is reduced from 2.26 K to 0.8 K (see Figure 8), which significantly improves the temperature uniformity of the

loading surface and significantly reduces the deformation and stress of the detector chip.

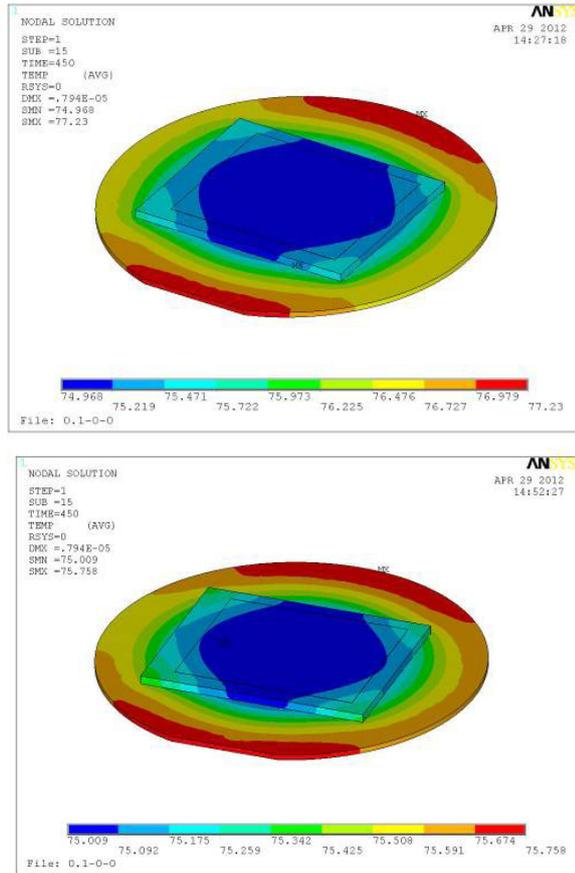


Figure 8. Cold head temperature distribution before and after Dewar design improvement

3. Component Performance and Environmental Test

Developed Ge based medium wave 1280×1024 focal plane detector is packaged in metal dewar and connected with Stirling refrigerator. The photoelectric performance of the module is tested. The main technical indexes are: working temperature 81 K, average NETD 18.5 mK, non-uniformity 7.5% and bad pixel rate 1.27%.

The environmental adaptability of the module is studied. The environmental test includes high-temperature storage, low-temperature storage, high-temperature impact, low-temperature impact, high-temperature work, low-temperature work, mechanical impact and impact. Specific environmental tests are as follows:

High temperature storage: storage temperature +71 °C for 24 h.

Low temperature storage: storage temperature -54 °C for 24 h.

High temperature operation: temperature +71 °C, heat

preservation for 1 h, operation for 2 h, and the temperature change rate shall not exceed 10 °C/min.

Low temperature operation: temperature -40 °C, heat preservation for 1h, operation for 2 h, and the temperature change rate shall not exceed 10 °C/min.

Temperature shock: low temperature -54 °C± 2 °C, high temperature + 71 °C± 2 °C, limit temperature maintained for 2 h, cycle for 3 times, and conversion time no more than 5 min.

Vibration: The component fulfills the specification during and after exposure to vibration in three mutually perpendicular axes during one hour per axis, with the following random profile to 5.33 g RMS. Between 5 Hz and 28 Hz, linear from 0.0026 g²/Hz to 0.08 g²/Hz. Between 28 Hz and 250 Hz, constant 0.08 g²/Hz. Between 250 Hz and 2000 Hz, linear from 0.08 g²/Hz to 0.00016 g²/Hz. See Figure 9.

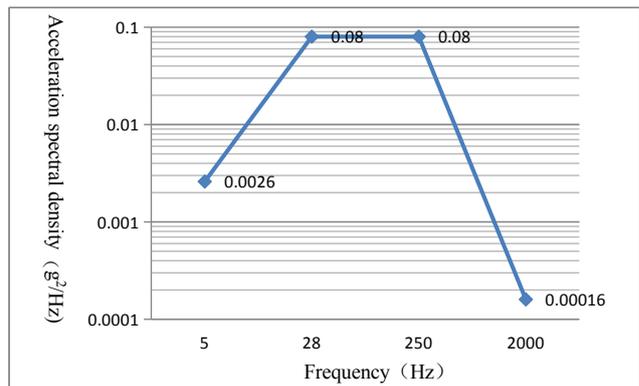


Figure 9. Random Vibration spectra

Mechanical shocks: The component fulfills the specification after exposure to shocks in each of the three mutually perpendicular axes with the following levels: 1/2sine 100 g 1 ms, with 3 shocks per axis per direction.; 1/2sine 50 g 6 ms, with 3 shocks per axis per direction; 1/2sine 40 g 18 ms, with 3 shocks per axis per direction; 1/2sine 25 g 6 ms, with 500 shocks per axis per direction.

The environmental test includes high-temperature storage, low-temperature storage, high-temperature impact, low-temperature impact, high-temperature work, low-temperature work, mechanical impact and shock. After the environmental test, the component performance has not changed significantly. At the same time, the performance of the components stored in the conventional environment for one year was retested, and there was no decline in performance.

4. Results & Discussion

In this paper, Ge substrate is used as the substrate of HgCdTe molecular beam epitaxy material, which replaces

CdZnTe substrate as the epitaxial substrate of HgCdTe material. Due to the high requirements of HgCdTe epitaxial film on the substrate, although CdZnTe and HgCdTe have small lattice mismatch coefficient, due to the low single crystal crystallization rate of CdZnTe and small ingot diameter. In particular, it is difficult to meet the requirements of large material substrate for large array HgCdTe infrared focal plane devices. At the same time, the growth cycle of CdZnTe crystal is long, about 40 days. Therefore, in the focal plane detector chip based on the traditional CdZnTe substrate, the qualified CdZnTe substrate accounts for the main cost of the detector chip. The production of HgCdTe thin film material by molecular beam epitaxy on Ge substrate has the advantages of low growth cost and short growth cycle. Therefore, using Ge based substrate instead of CdZnTe Single Crystal is expected to reduce the comprehensive cost of large area array infrared focal plane chip by more than 50%.

The above research results and related process methods can be applied to different specifications of Ge based medium wave array focal plane detector components. At the same time, it can also consider using Si substrate of the same material as readout circuit as the alternative substrate of CdZnTe to realize the preparation of low-cost infrared detector.

Conflicts of Interest

The authors declare that they have no conflicts of interest to report regarding the present study.

References

- [1] Nelms, N., Minoglou, K., Voland, C., et al., 2015. Visible and infrared detector development supported by the European Space Agency. Proceedings of SPIE. 9639, 96390O.
- [2] Yang, J.R., 2012. Physics and technology of HgCdTe materials. Beijing: National Defense Industry Press.
- [3] Li, Y.H., Yang, Ch.Zh., et al., August 2015. Molecular beam epitaxy CdTe films on 4-inch Ge substrates The 11th National molecular beam epitaxy conference.
- [4] Yang, Ch.Zh., Li, Y.H., et al., August 2015. Pretreatment of 3-inch Ge (211) substrate for MBE growth. 2015 academic conference of China Optical Society.
- [5] He, L., Yang, D.J., Ni, G.Q., et al., 2011. Introduction to advanced focal plane technology. Beijing: National Defense Industry Press.
- [6] Tian, L.P., Zhu, Y.F., Liu, X.Y., et al., 2013. Infrared technology. 35(10), 629-631.